Exploring the Use of the Finite Element Method for Electromigration Analysis in Future Physical Design

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***Abstract*—Addressing electromigration (EM) during physical design has become crucial to ensure reliable integrated circuits. Simulation methods, such as the finite element method (FEM), are increasingly overwhelmed by the complexity of the task. With further technology scaling, it is predicted that FEM will not be usable anymore for a full-chip EM analysis due to complexity reasons. To address this bottleneck, we present a new methodology of FEM-based full-chip EM analysis for future technologies down to 10 nanometer feature sizes. Our solution reduces analysis costs significantly by establishing pre-validated layout patterns without loosing accuracy of the verification results. Our full-chip meta-model EM analysis allows speedups of at least 10X compared to current FEM-based verification methods.**

I. Introduction

Excessive current density within interconnects is a major concern for integrated circuit (IC) designers because it causes electromigration (EM). Due to smaller feature sizes, this is a growing reliability issue in modern ICs [1]. While analog designers have been aware of this issue for some time, digital designs are now being affected as well [2], [3].

EM is a migration process mostly driven by momentum transfer between electrons and metal ions of the wire. It causes damage through formation of voids and hillocks. While directly depending on current density, damage takes place mostly in locations of inhomogeneous electric currents, such as vias or non-linear wiring shapes.

EM analysis by simulation helps to find excessive current densities in the layout. Hence, current-density verification has emerged as an important verification step in VLSI physical design. The most common method of analysis is the finite element method (FEM). While it has been widely accepted in analog layout verification, using FEM in significantly more complex digital circuits faces numerous challenges.

FEM uses meshes for discretization of arbitrary shapes of continuous matter. Each node and element of the mesh has its degrees of freedom to contribute to a linear system of differential equations. Therefore, the size of this system of equations and also calculation time depends on the number of nodes in the mesh.

Digital integrated circuits usually include a large number of transistors and nets. Additionally, current densities are growing with decreasing feature sizes [1]. To make matters worse, current density limits are also shrinking due to smaller structure sizes (Figure 1 and Section II).

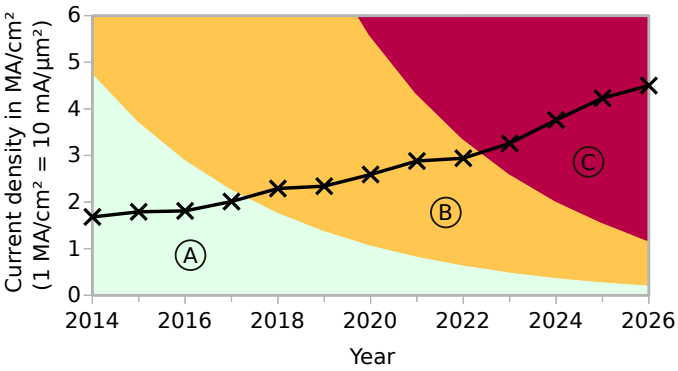

Figure 1. Expected evolution of required current density for driving four inverter gates for leading edge technologies according to ITRS roadmap [1]. As also shown, the maximum tolerable current density limits are shrinking due to smaller structure sizes. Region A / green: local EM issues, region B / yellow: all wires EM-affected, region C / red: no EM-solutions known yet.

As stated by [1], all minimum-sized wires in integrated circuits will be EM-affected after 2018. Subsequently, all wiring elements (segments, vias) of these circuits must be subjected to EM verification and analysis; totaling billions of elements for some circuits.

As FEM is commonly used for detailed analyses, the complexity of future circuits will demand excessive calculation cost. For full-chip analysis, other simulation methods are more time-efficient, but with the drawback of less detailed results and information loss in terms of potential void locations, for example. To the authors' knowledge, only FEM and similar methods such as the finite-difference method (FDM), possess the capability of spatially resolved analysis to visualize excessive current densities.

FEM-based verification will only be usable in the future if we achieve a significant reduction in simulation time. To meet this demand, we propose a new methodology that reduces simulation time at least tenfold by using FEM for pre-layout pattern analysis without accuracy loss.

II. The Need for EM Analysis

Size reduction of semiconductor structures is mainly driven by the need for higher circuit performance, efficiency at higher

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frequencies and smaller footprints. Furthermore, line widths and wire cross-sectional areas decrease over time to meet routing requirements of semiconductors. Table I shows that the cross-sectional area of Metal 1 shrinks from $1{,}600\,\mathrm{nm}^2$ in 2016 to roughly $600\,\mathrm{nm}^2$ in 2020. Although currents are decreasing as well due to shrinking gate capacitances and supply voltages (see Table I), current densities increase because of the significantly larger decrease of cross-sectional areas.

To make matters worse, smaller feature sizes also limit the maximum tolerable current densities, because small material defects will cause a dramatic change in resistance or even damage of the wires. As a result, maximum tolerable current densities must decrease to maintain a constant reliability [1], [2]. The ITRS [1] indicates that all minimum-sized interconnects will be EM-affected by 2018. Therefore, any further downscaling of wire sizes is increasingly restricted by current density constraints (marked by the yellow region B in Figure 1).

Taking into account that the total interconnect length per IC will continue to increase, reliability requirements per length unit of the wires need to increase in order to maintain overall IC reliability. However, the future decrease in interconnect reliability due to EM – as noted above – conflicts with these requirements. As the ITRS states that there are no known solutions to meet the EM-related reliability requirements of technologies in approximately 5 years from now (Figure 1, red region C), there is a strong need for time-efficient, full-chip EM analysis.

Table I
TECHNOLOGY PARAMETERS BASED ON THE ITRS, 2013 EDITION [1]; MAXIMUM CURRENTS AND CURRENT DENSITIES FOR COPPER AT 105 °C

Year	2016	2018	2020	2022	2024	2026
Gate Length (nm)	15.34	12.78	10.65	8.88	7.4	6.16
On-chip local clock frequency (GHz)	4.555	4.927	5.329	5.764	6.234	6.743
DC equivalent maximum current (µA)*	29.09	23.19	16.52	12.40	10.00	7.90
Metal 1 properties						
Width – halfpitch (nm)	28.35	22.50	17.86	14.17	11.25	8.93
Aspect ratio	2.0	2.0	2.0	2.1	2.1	2.2
Layer thickness (nm)*	56.70	45.00	35.72	29.76	23.63	19.65
Cross sectional area (nm^2)*	1607.4	1012.5	638.0	421.7	265.8	175.5
DC equivalent current densities ($\mathrm{MA/cm}^2$)						
Maximum current density without EM degradation**	3.0	1.8	1.1	0.7	0.4	0.3
Maximum current density (solution unknown)**	15.4	9.3	5.6	3.4	2.1	1.2
Required current density for driving four inverter gates	1.81	**2.29**	**2.59**	**2.94**	**3.76**	**4.50**

*) Calculated values, based on given width W, aspect ratio A/R, and current density J in [1], as follows: layer thickness $T = A/R \times W$, cross-sectional area $A = W \times T$ and current $I = J \times A$.
**) Approximated values from the ITRS Figure INTC9 [1].
All remaining values are from the ITRS 2013 edition [1].

III. Finite Element Method for EM Analysis

A. General Approach for EM Analysis

The finite element method can help analyzing the EM susceptibility by different approaches. The most obvious application of FEM in EM analysis is the calculation of current densities. As it is impracticable to calculate current densities analytically, the use of finite elements enables to lower the calculation costs. Current densities are calculated by solving the linear field equation for the electric field under voltage or current boundary conditions [4].

Nevertheless, not only current density influences migration. Also temperature and, at small feature sizes, mechanical stress must be considered in the simulation. This multi-physics problem is described by the diffusion equation [5] and results in an atomic flux under electromigration, thermomigration and mechanical stress as in

$$J_{\mathrm{total}} = J_{\mathrm{EM}} + J_{\mathrm{TM}} + J_{\mathrm{SM}}, \tag{1}$$

where J_{total} is the whole mass flux, and J_{EM}, J_{TM}, J_{SM} describe the mass flux caused by electromigration, thermomigration and stress migration, respectively.

Diffusion can be determined using quasi-static simulation by calculating the initial atomic flow. Lifetime and robustness will be estimated by extrapolation of this flow.

The applicability of finite element models for simulating migration processes and void growth until failures occur has been shown in [6], [7]. However, those simulations are very time-consuming and therefore not applicable to a full-chip EM analysis in VLSI physical design.

B. Benefits of FEM

As already indicated, FEM has great benefits compared to other techniques that simulate faster. In contrast to lumped element simulations, FEM offers simulation results with spatial resolution. This information is especially important when dealing with problems like EM, which cause failures by local damage. At the same time, FEM is more flexible and less time-consuming than analytic or continuous methods, when dealing with complex geometries. By scaling of the elements' size, calculation effort can be optimized depending on accuracy requirements.

C. Application in Physical Design

Current physical design tools such as [8]–[10] have built-in functionality for current density and, thus, EM analysis. Most analysis tools are based on the finite element method for calculating current density and temperatures. Still, those practical CAD applications only implement a small portion of

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the capability FEM tools used in other disciplines possess. Mostly, they use single-physics elements due to limitation of computing time. These tools cannot consider all effects connected with EM, such as mechanical stress and temperature gradients.

Analog designers make extensive use of the offered analysis tools. In digital designs, the available tools are increasingly limited to power and ground nets due to the excessive number of signal nets. Some authors, e.g. in [11], propose filter functions to address this complexity problem. Those filters rely on the availability of current information for all nets. This, and the fact that all nets become potentially critical in future digital designs, limit the use of the mentioned filters. As a result of this increase in verification complexity, FEM will no longer be usable for full-chip current density calculation.

IV. Problem Formulation: Limitations of FEM

A. Model Size Restriction

More and more nets are becoming EM-affected in digital designs [1], while at the same time design complexity increases due to down-scaling. It is practically impossible to use FEM for digital full-chip analysis. Based on the ITRS roadmap, Figure 2 shows a prediction of the analysis problem complexity for future digital circuits.

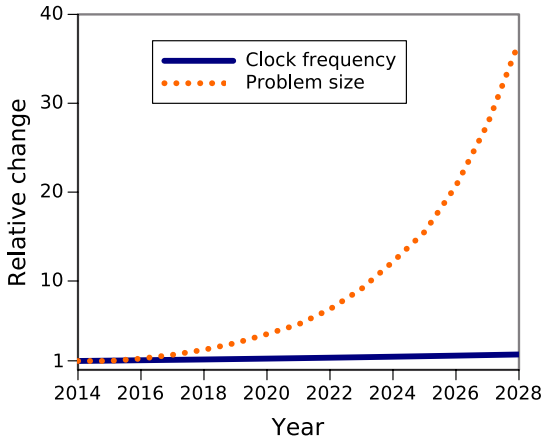

Figure 2. Complexity of finite element simulations of all signal nets in future technologies, as predicted by the ITRS relative to 2014. The respective clock frequency of CPUs is also depicted for comparison. Calculated from ITRS [1].

FEM works with meshed geometric models, where physical properties are assigned to discrete nodes and elements. Generally, precision and calculation time of FEM problems depend on model size, i.e. on the number of nodes and elements of the mesh. To gain a result in a given time, model size has to be limited. Precision demands a certain number of nodes per volume, therefore, the simulated volume per FE model has to be restricted.

FEM is limited to small portions of a layout. Hence, critical layout areas have to be identified and filtered. However, filters, like those proposed in [11], will no longer mitigate the complexity problem. Hence, FEM will not be usable anymore, as simulation cost would grow enormously.

Due to the large scale of whole chip models, the number of sub-models used in FEM will increase with technology progress. To limit this increase, we suggest the use of re-usable sub-models. That means, *standardized* sub-units of the interconnect structure have to be established and re-used. This leads to a layout composed of a large number of few, pre-determined basic building blocks in terms of interconnect structures that would facilitate the FEM analysis. The gained efficiency for EM verification from our approach increases with growing layout complexity.

B. Atomic Scale Restriction

Further downscaling imposes limitations due to influences of the atomic scale. At feature sizes in the range of 4 to 5 nanometers, single atoms affect the failure probability, i.e., if there is a failure or not. Hence, the wire cannot be regarded as a continuum. The violation of this fundamental demand for FEM disallows further use of this method in those size ranges. When going near this point, strong inhomogeneities may occur. These can be dealt with by using non-linear models for EM calculation as it has been applied to different other inhomogeneities on a micro scale. Hence, our approach is restricted to all technologies with a metal pitch not smaller than 10 nm.

V. Our Approach: Pattern Verification

Our approach uses the advantages of FEM without the necessity of large models or a great number of smaller FE models consuming a lot of computing power. The basic principle is to simulate patterns of wire structures that are used for routing afterwards. Layout patterns with a high repetition rate in layout, i.e., that are common, have to be determined and pre-simulated. Hence, simulation costs of the final layout verification can be significantly reduced (see Section VI-C).

A. Basic Principle

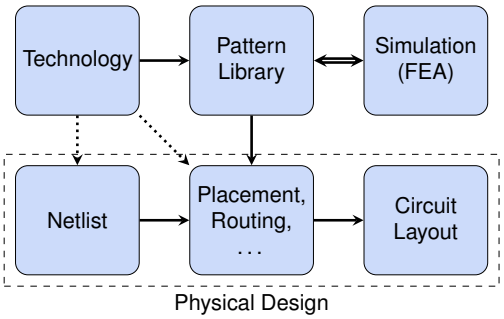

Figure 3. Layout synthesis using our proposed pattern verification method.

We propose a pre-layout simulation of metalization patterns and the restriction of routing to those simulated patterns. Our method is based on the following (Figure 3):

- Technology restrictions will be taken into account for FE simulation.
- All common patterns needed for interconnection analysis are generated and simulated by FEM.

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- These pre-defined layout patterns comprise typical wiring elements, such as via connections, long and short wires, and in-layer junctions (T-shaped or crossing).
- The EM robustness of the patterns for individual current constraints is verified by simulation.
- Routing is performed using wiring patterns suitable for particular currents of the nets.

While these measures alone cannot guarantee a reliable design, they are the foundation to enable a full-chip verification to ensure circuit reliability (see subsequent sections).

B. Pattern Choice

The requirements for deducing a full-chip verification from the verification of all its elements are as follows:

- currents should be equally distributed at model boundaries,
- temperature influences and mechanical stress from the neighborhood should be negligible, and
- diffusion at the boundaries should be known or zero.

The last point is easily satisfiable if model boundaries with current flow are always at the boundary between different materials, e.g. at tungsten plugs connecting to silicon or metal-via interfaces containing diffusion barriers. However, the first requirement is not fulfilled in this case, as the interfaces are always near current crowding regions due to turns of the current direction from horizontal to vertical or vice versa. By adding geometric appendices to the model at such boundaries, the correct current distribution at the boundary can be achieved while the results inside the appendix are ignored.

Mechanical and thermal influences are harder to neglect, as they do not only influence a pattern or segment from two sides but they take effect from all around the simulation model. Both temperature and mechanical stress are transmitted through the surrounding dielectric material.

C. From Pattern Verification to Full Chip Verification

We will show how FE simulations can be performed without knowing the surrounding of a wiring pattern, as this is always the case when running a simulation prior to routing. A successful verification using a limited number of FE simulation is based on one of the following constraint assumptions:

1) A worst case analysis (all patterns are verified for the largest current in the circuit) is performed, where only the constraints have to be verified for the full-chip verification. This leads to robust, but over-sized designs.
2) An average estimation of constraints (FE simulations for typical loads) is performed. This can lead to partially unreliable systems.
3) The exact constraints are calculated. This is not feasible in pre-layout analysis.
4) New estimation metrics for constraints based on known current values are used. This approach works with meta-models of the design patterns that can be used in a full-chip analysis using concentrated elements.
5) Different variants of the same pattern type are simulated, where a certain pattern can be selected from the library depending on actual constraints.

The approach 4) using meta-models is the most promising. It demands some additional simulation time during or after routing, but this time is limited due to the use of simple models. The proposed meta-models are mathematical relations between FE model constraints and result quantities, e.g. maximum current density. Additional constraints to be implemented are current values (from circuit simulation) and hydrostatic stress. As a first implementation, both are only propagated at the electrically conducting boundaries between neighboring interconnect patterns. Therefore, a limited amount of additional simulation data is created.

When proceeding to smaller scale, it might also become necessary to propagate hydrostatic stress between wiring elements that are not electrically connected. Here lies the limitation of this approach, because the full-chip model complexity will then increase comparably to interconnect simulation models incorporating capacitive crosstalk.

Given the before mentioned circumstances, the pattern analysis allows a reliability prediction of the entire wiring structure.

VI. Results

We choose the following method in order to verify our approach: Firstly (A), we show that partitioning FE models of the wiring is possible without losing accuracy of the current density results. Secondly (B), we present an application on full-chip examples to illustrate the scaling effect. Thirdly (C), the reduction in calculation time is estimated based on technology data.

A. Example Simulations for Patterns and Their Combination

It is important to verify that partitioning FE models of wiring is possible without losing accuracy of the current density results. This is done by comparing the simulation results of generic sample patterns calculated both separately and in combination. Different manually generated patterns from a generic technology have been analyzed. As an example, a T-shape inside one metal layer and a via connection are chosen. Figure 4 shows the current density results from two separate (distinct) simulations.

For comparison, the combination of these patterns is used in a second simulation (Figure 5). The simulation results of the combined configuration show a good correspondence to the separately calculated results.

Figure 6 indicates current density distribution at the interface between the two patterns in the common simulation, which is a measure for the error in the separate simulations. The maximum error is 3 % in our case; this value has been verified for the other patterns (see Figure 7) as well.

Hence, under the constraints mentioned in Section V-C, simulation time can be reduced significantly by splitting an FE model into smaller parts while preserving the accuracy of the results.

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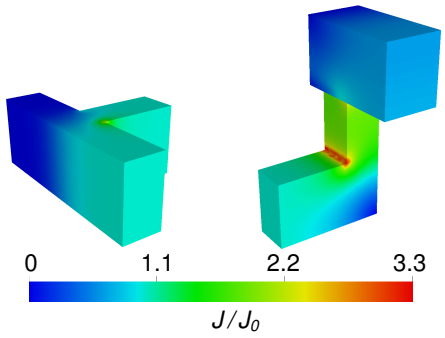

Figure 4. Results of the separate simulations of single patterns with homogeneous constraints at the cut surfaces.

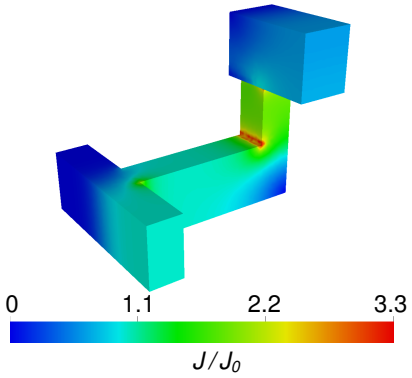

Figure 5. The results of the common simulation of the two patterns show a good similarity with the results of the separate simulations from Figure 4.

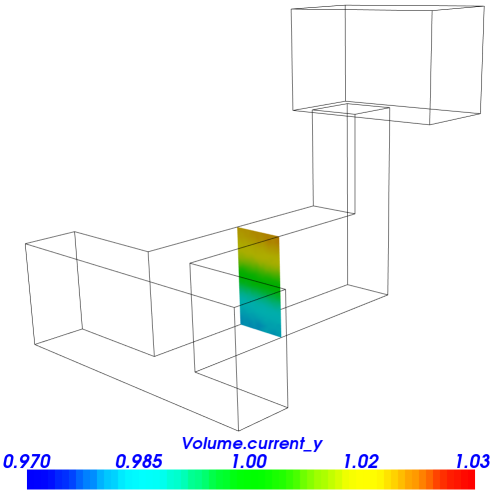

Figure 6. Verifying homogeneity of the current density at the cut surface between the two sub-models (3 % maximum deviation here) ensures that distinct and combined simulations show matching results.

Figure 7. Typical, pre-defined wiring and via patterns that have to be simulated by FEM in addition to those from Figure 4.

B. Full-Chip Analysis

We chose layouts (Figure 8) from the MCNC benchmark suite[1] for verification and analyzed it in two ways:

1) FE simulation of the complete circuit *(full-chip, F)* and
2) partitioned simulation re-using repeated patterns *(partitioned, P)*.

The first approach produces very large simulation models with $N_\mathrm{F} > 10^7$ nodes and excessive simulation times $t_\mathrm{F} > 70\,\mathrm{h}$. We can safely assume that FE simulation will be impossible with larger layouts in reasonable time. The second approach uses predefined and verified patterns (compare Figures 4 and 7). An algorithm to localize the defined patterns has been implemented and applied to the benchmark layouts (Figure 8). By reusing the patterns, the problem size is reduced to a significantly lower number of nodes N_P enabling a reduced simulation time t_P. Please note that by improving pattern choice, N_P can be reduced further.

Full-chip simulation time t_F is compared directly with simulation time t_P of the partitioned approach (Table II).

The overall calculation time can be estimated by

$$t_\mathrm{F} \approx P_\mathrm{C} \cdot t_1 \text{ and} \quad (2)$$

$$t_\mathrm{P} \approx P_\mathrm{L} \cdot t_1 + P_\mathrm{C} \cdot t_\mathrm{m}, \quad (3)$$

[1]The MCNC benchmark suite was originally obtained from [12] and adjusted to contain only single vias as outlined in [13].

with the number of patterns per circuit P_C, the mean calculation time for FE simulation of a single pattern t_1, the number of patterns in a library P_L, and the mean calculation time for a pattern meta-model t_m.

All critical spots of the full-chip analysis can be detected using only 5 different patterns (see Figure 7). As shown, simulation time can be reduced by a factor of at least 16 (Table II). Please note that library buildup time, i.e., FE simulation of individual patterns, is included in our simulation time.

N_P is always 30,000 as similar pattern libraries are used for all benchmarks. Numbers of nodes and calculation times are estimated based on wire length and number of patterns in the layout (see Figure 8). t_P includes the estimated meta-model evaluation time (see equation 3).

A larger pattern library can be worthwhile if a large number of layouts is to be analyzed, reducing the simulation time per layout even further.

C. Reduction in Simulation Time

The time needed for simulation using the pattern method comprises (a) the time needed for library buildup (FE simulation of individual patterns) and (b) the full-chip meta-model calculation time. The FE simulation of individual patterns (a) is only necessary once for a variety of similar circuits.

For a number P_L of patterns in a library, the proposed method results in a reduced simulation time compared to full

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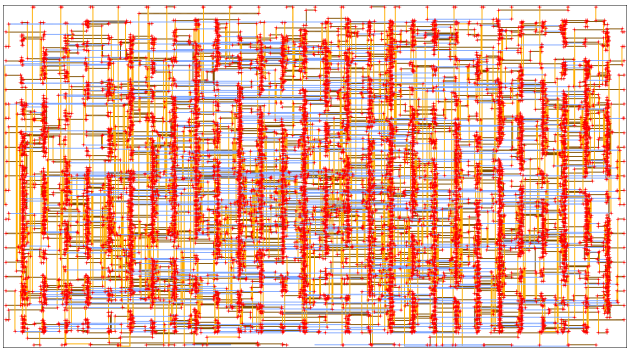

Figure 8. Layout of the benchmark circuit *s5378*. Red crosses note the location of the example patterns of Figure 7.

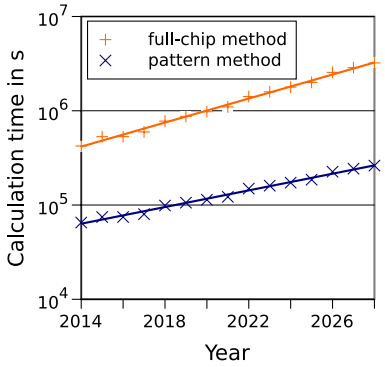

Figure 9. Comparison of estimated calculation times between full-chip analysis and pattern method for $s = 1$ (one circuit verification per pattern library), calculated from technology parameters from [1].

Table II
EXPERIMENTAL RESULTS OF THE LAYOUTS OF THE MCNC BENCHMARK SUITE.

#	Benchmark name	full-chip		partitioned	
		N_F	t_F	t_P	Speedup
1	mcc1	3.8×10^7	106.2 h	3.4 h	31.6 ×
2	mcc2	4.0×10^8	1,106.8 h	19.5 h	56.6 ×
3	primary1	5.0×10^7	138.4 h	3.6 h	39.0 ×
4	primary2	2.0×10^8	569.8 h	14.5 h	39.2 ×
5	struct	5.6×10^7	154.6 h	5.5 h	28.2 ×
6	s13207	6.7×10^7	186.3 h	10.7 h	17.4 ×
7	s15850	8.0×10^7	221.9 h	12.7 h	17.5 ×
8	s38417	2.0×10^8	543.2 h	31.4 h	17.3 ×
9	s38584	2.6×10^8	728.1 h	41.8 h	17.4 ×
10	s5378	3.0×10^7	83.9 h	4.9 h	17.1 ×
11	s9234	2.5×10^7	70.1 h	4.2 h	16.7 ×

chip analysis if $t_\mathrm{P}(s) < t_\mathrm{F}(s)$ or:

$$P_\mathrm{L} \cdot t_1 + s \cdot P_\mathrm{C} \cdot t_\mathrm{m} < s \cdot P_\mathrm{C} \cdot t_1, \tag{4}$$

with s the number of similar circuits to be analyzed.

That means, the approach accelerates the analysis if both the library contains much less patterns than a circuit and FE simulation time is greater than meta-model evaluation time. Due to increasing influences between model partitions with further downscaling of feature sizes, the number of patterns and the calculation time will rise. Figure 9 shows the difference in calculation time for $s = 1$, i.e., the pattern library is only used once (worst-case), illustrating nevertheless a speedup of at least 10 for current and future technologies.

If the library models can be used multiple times for one circuit or if analyzing several similar circuits, i.e., $s > 1$, the difference between calculation times becomes even more significant. Specifically, when looking at the overall analysis time for large numbers of circuits, a speedup of at least 50 can be achieved, which nearly corresponds to the speedup of a meta-model calculation compared to an FE calculation.

VII. SUMMARY

The finite element method (FEM) is well established in physical design and has shown good reliability for electromigration analysis. Downscaling of the dimensions in integrated circuits leads to increasing problems with electromigration which needs to be tackled with greater awareness and more analyses.

Since FEM will lose the battle against circuit complexity, an alternative strategy is presented. Our approach uses FEM only for calculating generic layout elements (patterns) in advance to build a meta-model library. The layout will be created from a variety of library patterns, enabling a simple meta-model EM analysis. We verified our method using layouts of the MCNC benchmark suite and showed an acceleration of EM analysis by a factor of at least 16.

Further work will investigate the practical implications of complex, nano-scale layout synthesis that is based on the use of library patterns.

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